IN THE CLAIMS:

Each of claims 3–6, 9, 10, 21–24 and 27–32 has been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1 and 2 (cancelled).

Claim 3 (currently amended) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, ~~said~~the intermediate structure further including at least one transistor gate member spanned between ~~said~~the at least one implanted drain region and ~~said~~the at least one implanted source region on ~~said~~the at least one active area;

a first barrier layer planarized down to ~~said~~the at least one transistor gate member and substantially covering ~~said~~the at least one thick field oxide ~~area, said~~area and the at least one active area, and adjacent ~~said~~the at least one transistor gate member;

at least one drain contact plug extending through ~~said~~the first barrier layer, wherein ~~said~~the at least one drain contact plug is in electrical communication with ~~said~~the at least one implanted drain region on ~~said~~the ~~semiconductor~~ substrate;

at least one source contact plug extending through ~~said~~the first barrier layer, wherein ~~said~~the at least one source contact plug is in electrical communication with ~~said~~the at least one implanted source region on ~~said~~the ~~semiconductor~~ substrate;

an individual drain contact land disposed atop ~~each of said~~the at least one drain contact ~~plugs~~ plug and a portion of ~~said~~the first barrier layer, ~~said~~the individual drain contact land wider than ~~said~~the at least one drain contact plug;

an individual source contact land disposed atop ~~each of said~~the at least one source contact ~~plugs~~ plug and a portion of ~~said~~the first barrier layer, ~~said~~the individual source contact land wider than ~~said~~the at least one source contact plug;

a second barrier layer disposed over ~~said~~the first barrier layer, ~~said~~the individual drain contact land, and ~~said~~the individual source contact land;

at least one upper source contact extending through ~~said~~the second barrier layer, ~~said~~the at least one upper source contact in electrical communication with ~~at least one of said~~the individual source contact ~~lands~~land; and

at least one upper drain contact extending through ~~said~~the second barrier layer, ~~said~~the at least one upper drain contact in electrical communication with ~~at least one of said~~the individual drain contact ~~lands~~land.

Claim 4 (currently amended) The transistor of claim 3, further comprising drain contact metallization in electrical communication with ~~said~~the at least one upper drain contact; and source contact metallization in electrical communication with ~~said~~the at least one upper source contact.

Claim 5 (currently amended) The transistor of claim 3, wherein ~~said~~the at least one source contact plug extends between at least two source regions.

Claim 6 (currently amended) The transistor of claim 3, wherein ~~said~~the at least one drain contact plug extends between at least two drain regions.

Claim 7 and 8 (cancelled).

Claim 9 (currently amended) The transistor of claim 3, wherein ~~said~~the at least one upper source contact extends between at least two individual source contact lands.

Claim 10 (currently amended) The transistor of claim 3, wherein ~~said~~the at least one upper drain contact extends between at least two individual drain contact lands.

Claims 11 through 20 (cancelled).

Claim 21 (currently amended) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, ~~said~~the intermediate structure further including at least one transistor gate member spanned between ~~said~~the at least one implanted drain region and ~~said~~the at least one implanted source region on ~~said~~the at least one active area;

a first barrier layer planarized down to ~~said~~the at least one transistor gate member and substantially covering ~~said~~the at least one thick field oxide area, ~~said~~the at least one active area, and adjacent ~~said~~the at least one transistor gate member;

at least one drain contact plug extending through ~~said~~the first barrier layer, wherein ~~said~~the at least one drain contact plug is in electrical communication with ~~said~~the at least one implanted drain region on ~~said~~the semiconductor substrate;

at least one source contact plug extending through ~~said~~the first barrier layer, wherein ~~said~~the at least one source contact plug is in electrical communication with ~~said~~the at least one implanted source region on ~~said~~the semiconductor substrate;

an individual drain contact land disposed atop ~~said~~the at least one drain contact plug and a portion of ~~said~~the first barrier layer, ~~said~~the individual drain contact land wider than ~~said~~the at least one drain contact plug;

an individual source contact land disposed atop ~~said~~the at least one source contact plug and a portion of ~~said~~the first barrier layer, ~~said~~the individual source contact land wider than ~~said~~the at least one source contact plug;

a second barrier layer disposed over ~~said~~the first barrier layer;

at least one upper source contact extending through ~~said~~the second barrier layer, ~~said~~the at least one upper source contact in electrical communication with ~~at least one said~~the individual source contact land; and

at least one upper drain contact extending through ~~said~~the second barrier layer, ~~said~~the at least one upper drain contact in electrical communication with ~~at least one said~~the individual drain contact land.

Claim 22 (currently amended) The semiconductor device of claim 21, further comprising drain contact metallization in electrical communication with ~~said~~the at least one upper drain contact; and source contact metallization in electrical communication with ~~said~~the at least one upper source contact.

Claim 23 (currently amended) The semiconductor device of claim 21, wherein ~~said~~the at least one source contact plug extends between at least two source regions.

Claim 24 (currently amended) The semiconductor device of claim 21, wherein ~~said~~the at least one drain contact plug extends between at least two drain regions.

Claims 25 and 26 (cancelled).

Claim 27 (currently amended) The semiconductor device of claim 21, wherein ~~said~~the at least one upper source contact extends between at least two individual source contact lands.

Claim 28 (currently amended) The semiconductor device of claim 21, wherein ~~said~~the at least one upper drain contact extends between at least two individual drain contact lands.

Claim 29 (currently amended) A contact for a semiconductor device, comprising:

a single contact plug extending through a first barrier layer and a second barrier layer, ~~said~~the second barrier layer disposed over ~~said~~the first barrier layer and planarized down to a transistor gate member, ~~said~~the single contact plug being in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop ~~said~~the single contact plug and a portion of ~~said~~the second barrier layer, wherein ~~said~~the individual contact land is wider than ~~said~~the single contact plug; and

an upper contact extending through a third barrier layer, ~~said~~the third barrier layer disposed over ~~said~~the second barrier layer, to form an electrical contact with ~~said~~the individual contact land.

Claim 30 (currently amended) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, ~~said~~the intermediate structure further including at least one transistor gate member spanned between ~~said~~the at least one implanted drain region and ~~said~~the at least one implanted source region on ~~said~~the at least one active area;

a first barrier layer substantially covering ~~said~~the at least one thick field oxide area and ~~said~~the at least one active area, and adjacent ~~said~~the at least one transistor gate member;

a second barrier layer disposed over ~~said~~the first barrier layer and planarized down to ~~said~~the at least one transistor gate member;

at least one drain contact plug extending through each of ~~said~~the first and second barrier layers, wherein ~~said~~the at least one drain contact plug is in electrical communication with ~~said~~the at least one implanted drain region on ~~said~~the ~~semiconductor~~ substrate;

at least one source contact plug extending through each of ~~said~~the first and second barrier layers, wherein ~~said~~the at least one source contact plug is in electrical communication with ~~said~~the at least one implanted source region on ~~said~~the ~~semiconductor~~ substrate;

an individual drain contact land disposed atop ~~each of said~~the at least one drain contact ~~plugs~~ plug and a portion of ~~said~~the second barrier layer, ~~said~~the individual drain contact land wider than ~~said~~the at least one drain contact plug;

an individual source contact land disposed atop ~~each of said~~the at least one source contact ~~plugs~~ plug and a portion of ~~said~~the second barrier layer, ~~said~~the individual source contact land wider than ~~said~~the at least one source contact plug;

a third barrier layer disposed over ~~said~~the second barrier layer, ~~said~~the individual drain contact land, and ~~said~~the individual source contact land;

at least one upper source contact extending through ~~said~~the third barrier layer, ~~said~~the at least one upper source contact in electrical communication with ~~said~~the individual source contact land; and

at least one upper drain contact extending through ~~said~~the third barrier layer, ~~said~~the at least one upper drain contact in electrical communication with ~~said~~the individual drain contact land.

Claim 31 (currently amended) A semiconductor device including at least one contact, comprising:

a single contact plug extending through each of a first barrier layer and a second barrier layer, ~~said~~the second barrier disposed over ~~said~~the first barrier layer and planarized down to a transistor gate member, ~~said~~the single contact plug being in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop ~~said~~the single contact plug and a portion of ~~said~~the second barrier layer, ~~said~~the individual contact land being wider than ~~said~~the single contact plug; and

an upper contact extending through a third barrier layer, ~~said~~the third barrier layer disposed over ~~said~~the second barrier layer, to form an electrical contact with ~~said~~the individual contact land.

Claim 32 (currently amended) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, ~~said~~the intermediate structure further including at least one transistor gate member spanned between ~~said~~the at least one implanted drain region and ~~said~~the at least one implanted source region on ~~said~~the at least one active area;

a first barrier layer substantially covering ~~said~~the at least one thick field oxide area and ~~said~~the at least one active area, and adjacent ~~said~~the at least one transistor gate member;

a second barrier layer disposed over ~~said~~the first barrier layer and planarized down to ~~said~~the at least one transistor gate member;

at least one drain contact plug extending through each of ~~said~~the first and second barrier layers, wherein ~~said~~the at least one drain contact plug is in electrical communication with ~~said~~the at least one implanted drain region on ~~said~~the semiconductor substrate;

at least one source contact plug extending through each of ~~said~~the first and second barrier layers, wherein ~~said~~the at least one source contact plug is in electrical communication with ~~said~~the at least one implanted source region on ~~said~~the semiconductor substrate;

an individual drain contact land disposed atop ~~said~~the at least one drain contact plug and a portion of ~~said~~the second barrier layer, ~~said~~the individual drain contact land being wider than ~~said~~the at least one drain contact plug;

an individual source contact land disposed atop ~~said~~the at least one source contact plug and a portion of ~~said~~the second barrier layer, ~~said~~the individual source contact land being wider than ~~said~~the at least one source contact plug;

a third barrier layer disposed over ~~said~~the second barrier layer, ~~said~~the individual source contact land and ~~said~~the individual drain contact land;

at least one upper source contact extending through ~~said~~the third barrier layer, ~~said~~the at least one upper source contact being in electrical communication with ~~said~~the individual source contact land; and

at least one upper drain contact extending through ~~said~~the third barrier layer, ~~said~~the at least one upper drain contact being in electrical communication with ~~said~~the individual drain contact land.